REMARKS

- Claims 1, 2, 18, and 20 to 31 remain pending
- Claims 1, 18 and 24 are the only pending independent claims
- Claims 1, and 18 have been amended herein, no new matter has been added

I. DRAWING OBJECTION

The drawings stand objected to under 37 CFR 1.83(a) as not showing every feature of the invention specified in the claims. Specifically the Examiner objects to Claim 18 which recites the term "a computer." Applicants respectfully object to the Examiner's requirement because Applicants are not claiming "a computer" as a feature of the invention. Rather, Applicants claim "a medium readable by a computer" where the "medium readable by" is the claimed feature and "a computer" is merely inferentially referenced. Therefore, since a computer is not claimed, there should not be a requirement to show "a computer" in the drawings. Thus, Applicants respectfully request withdrawal of the Examiner's objection.

II. CLAIM REJECTIONS 35 U.S.C. § 112

Claims 1, 18, and 24 and their dependencies stand rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the enablement requirement. Applicants respectfully traverse these rejections.

Claims 1, 18, and 24 stand rejected as the Examiner contends "subset" finds no clear support in the specification. Applicants respectfully traverse the Examiner's rejection. Applicants are using the plain English meaning of the word "subset," namely, "a part of a larger group of related things." (see, e.g., Oxford English Dictionary, Third Edition, 23 June

2005) Throughout Applicants' specification, the concept of selecting only part of a larger group of latches in a circuit design is described. See for example, page 8, line 26 to page 9, line 14 wherein a method of selecting latches to treat as transparent is described. The selected latches are a subset of the larger group of all latches in a circuit design. Thus, no special meaning is attributed to the claim term "subset;" the concept is clearly described in the specification (albeit without using the particular term); and the specification supports the use of the term in the claims. Therefore, Applicants respectfully request withdrawal of the Examiner's rejection.

Claims 1, 18, and 24 stand rejected as the Examiner contends the limitation "allowing a selected subset of one or more latches of the circuit design to exhibit latch transparency while the selected subset is still being modeled as non-transparent by the timing tool" finds no clear support in the specification. Applicants respectfully traverse the Examiner's rejection. Applicants respectfully assert that the limitation, as it appears in Applicants' claims, is in fact supported in the specification. See, for example, at least page 2, lines 6 to 18 and page 8, lines 2 to 20:

> A delay value for local clock indicates the amount of time by which a rising (e.g., leading) edge of a launch clock signal input to a latch associated with the local clock is to be delayed. Delaying the rising (e.g., leading) edge of the launch clock signal input to a latch during circuit timing simulation allows the timing tool to effectively simulate circumstances in which data arrives at the latch after the rising edge of the launch clock but is nevertheless launched out of the latch (e.g., due to latch transparency) without the simulation resulting in an error condition. That is, because the launch clock signal input to the latch (e.g., the

> slave latch in a master-slave latch set) during the timing simulation is delayed, the timing tool treats the data that would otherwise arrive at the latch after the rising edge of the launch clock signal as if it arrives at the latch prior to the rising edge of the launch clock signal. Therefore, the timing tool does not generate an error condition. (Applicants' specification, page 8, lines 2 to 20)

Thus, Applicants' specification clearly describes a method of how a latch may be modeled as transparent: by "[d]elaying the rising (e.g., leading) edge of the launch clock signal input to a latch during circuit timing modeling."

Further, Applicants respectfully direct the Examiner's attention to Applicants' specification at page 7, line 30 to page 8, line 25. This passage of Applicants' specification explains that in some embodiments, Applicants' invention models latches as non-transparent but delays "the rising (e.g., leading) edge of the launch clock signal input to a latch during circuit timing simulation [which] allows the timing tool to effectively simulate circumstances in which data arrives at the latch after the rising edge of the launch clock but is nevertheless launched out of the latch (e.g., due to latch transparency) without the simulation resulting in an error condition." Page 8, lines 5 to 13. In other words, a latch can be made to exhibit latch transparency by delaying the rising edge of the launch clock signal input to the latch. This delaying of an input signal can be done to a latch that is being modeled as non-transparent. Thus, Applicants' specification provides clear support for this claim feature.

Still further, Applicants' specification clearly describes a method of how a latch may be modeled as non-transparent: "without including any delay values for local clocks." See, for example, at least page 9, lines 5 to 8: "a

circuit designer may perform an initial timing run on an integrated circuit without including any delay values for local clocks (e.g., with all latches being treated as non-transparent)."

Accordingly, applicants respectfully request withdrawal of the Examiner's rejections of claims 1, 18, 24, and their respective dependent claims.

Claims 1, 18, and 24 and their dependencies stand rejected under 35 U.S.C. § 112, second paragraph as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The rejections under this section are defined as A, B, and C in the current Office Action. Applicants respectfully traverse the Examiner's rejections.

A. The Examiner contends "non-transparent" and "transparent" are not clearly defined in claims 1, 18, and 24. The Examiner appears to be requiring that Applicants include additional limitations to Claims 1, 18, and 24 to define the terms "non-transparent" and "transparent." However, these terms are clearly defined throughout Applicants' specification. See, for example, at least page 2, lines 6 to 32. Further, the terms "non-transparent" and "transparent" are well known in the art and require no further definition. Applicants respectfully object to the Examiner's requirement given there is no basis in the law to require inclusion in the claims of such definitions. Thus, Applicants respectfully request withdrawal of the Examiner's rejection.

B. The Examiner contends the claim feature: "timing tool models each latch of the circuit design as being non-transparent" is an incomplete claim structure. Applicants respectfully traverse the Examiner's rejection. Applicants direct the Examiner to Applicants' Specification at Page 16, lines 1-14 and FIG. 3, where, contrary to the Examiner's

contention, Applicants clearly describe a non-limiting example of how a latch may be modeled as "non-transparent". Applicants respectfully assert that the quoted phrase as it appears in Applicants' claims is in fact complete and the meaning is clear, particularly in light of the specification. See, for example, at least page 9, lines 5 to 8: "a circuit designer may perform an initial timing run on an integrated circuit without including any delay values for local clocks (e.g., with all latches being treated as non-transparent)." Thus, Applicants' specification clearly describes a method of how a latch may be modeled as non-transparent: "without including any delay values for local clocks." The Examiner is respectfully reminded that Applicants are not required to recite definitions in the claims and that language that encompasses multiple methods may be used. Therefore, Applicants respectfully object to the Examiner's requirement to further narrow claims 1, 18, and 24 without providing a reference that discloses Applicants' invention as claimed. Absent such a reference, Applicants respectfully request withdrawal of the Examiner's rejection.

C. The Examiner contends the claim feature "allowing a selected subset of one or more latches of the circuit design to exhibit latch transparency while the selected subset is still being modeled as non-transparent by the timing tool" is an incomplete claim structure and is an unclear, conflicting, and contradicting limitation. As discussed above with respect to the § 112, first paragraph rejection, Applicants respectfully assert that the quoted phrase as it appears in Applicants' claims is in fact complete and the meaning is clear, particularly in light of the specification. Applicants further direct the Examiner's attention to Applicants' Specification at least at Page 16, lines 1-14 and FIG. 3, where, contrary to the Examiner's contention, Applicants clearly describe a non-limiting example of this claim feature.

For clarity, Applicants note that in this non-limiting example the quoted claim feature may be understood in view of FIG. 3 as follows:

"allowing a selected subset of one or more latches of the circuit design" (e.g., L2 latches 306, 312);

"to exhibit latch transparency" (e.g., "Because a delay 328 is added to the path of the data clock signal dclk (e.g., via a pair of inverters) in the hardware, dclk and lclk coupled to a latch (e.g., master/slave latch) may be overlapping during operation of the latch and therefore, the latch is treated as transparent." (Applicants' Specification, Page 16, lines 5-10));

"while the selected subset" (e.g., L2 latches 306, 312);

"is still being modeled as non-transparent by the timing tool" (e.g., "By delaying the leading edge of the lclk during modeling, the lclk and dclk may no longer overlap such that the latch is treated as non-transparent in the model" (Applicants' Specification, Page 16, lines 10-13)).

The Examiner contends it is unclear how a latch may exhibit latch transparency while being modeled as non-transparent by the timing tool. Applicants refer the Examiner at least to Applicants' Specification at Page 16, lines 5-14. Here, Applicants describe how, in a circuit, a delay may be added to the launch clock signal, which may overlap with the data clock signal. Some overlaps of the launch clock signal and data clock signal cause the timing tool to treat the latch as transparent. Please see Applicants' Specification with respect to FIG. 3. By delaying the leading edge of the data clock signal during modeling, the launch clock signal and data clock signal may no longer overlap such that the latch is treated as non-transparent in the model (e.g., the data arrives at the latch *after* the launch clock signal leading edge and is

delayed). Thus, the latch may be *modeled* as non-transparent based on a *modeled* delay in one or more clock signals (e.g., data clock signals) while one or more latches or a subset of these latches in a circuit may, in a normal function mode, actually exhibit latch transparency.

The Examiner further contends "[i]t is a conflicting and contradicting limitation as to how the same subset… can be modeled as transparent while (the selected subset) still being modeled as non-transparent." Applicants respectfully submit this is not what is claimed and directs the Examiner to the actual language of the claim. Specifically, claim 1 recites, among other things, "allowing a selected subset of one or more latches of the circuit design to exhibit latch transparency while the selected subset is still being *modeled* as *non-transparent* by the timing tool during modeling of a timing behavior of the circuit design with the timing tool." (emphasis added). Claims 18 and 24 recite similar features. The claims recite that a latch may exhibit latch transparency (e.g., the subset of latches may be transparent), but may be *modeled* (e.g., simulated) in a modeling operation as being non-transparent. Please see the above discussions regarding this feature for a detailed explanation.

Accordingly, as Claims 1, 18, 24 and their respective dependent claims are complete in that they particularly point out and distinctly claim that which Applicants regard as the invention, Applicants respectfully request the Examiner reconsider and withdraw the § 112 rejections.

Regarding the Examiner's rejections of Claims 1 and 18 on Page 4 of the current Office Action, Applicants have amended claims 1 and 18 to recite "the circuit design" in appropriate locations for clarity and proper antecedent basis. Accordingly, Applicants respectfully request the Examiner withdraw these rejections.

III. CLAIM REJECTIONS 35 U.S.C. § 102(b)

Claims 1-2, 18, and 20-31 stand rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,355,321 ("Grodstein"). Applicants respectfully traverse this rejection.

Applicants respectfully submit the Examiner previously rejected Applicants' claims based on Grodstein and, after Applicants arguments and clarifying amendments, allowed the claims. The present Office Action cites no new art nor does it include further reference to Grodstein beyond that previously presented.

Contrary to the Examiner's assertions, Grodstein does not appear to disclose the all features of the present invention. Specifically, Grodstein does not appear to show a method of "allowing a selected subset of one or more latches of the circuit design to exhibit latch transparency while the selected subset is still being modeled as non-transparent by the timing tool during modeling of a timing behavior of the circuit design with the timing tool", as recited in independent claim 1. Claims 18 and 24 recite similar claim features.

Applicants describe in the Specification at least at Page 8, lines 2-25 and Page 9, lines 8-13 an example of locally treating latches as transparent during modeling. Specifically, Applicants' Specification describes the method of allowing one or more latches of the circuit design to be locally treated as exhibiting latch transparency in that "the designer may easily add transparency to latches at a local level by specifying a delay value for the local clock that is coupled to the latches." Additionally, Applicants recite that "a selected subset of one or more latches" exhibit latch transparency. Accordingly, "every latch of the circuit design need not be treated as transparent during modeling." (Applicants'

Specification, Page 3, lines 28-29) Applicants respectfully submit the methods as claimed in independent claims 1 and 24 and the computer program product of independent claim 18 allow the user to select which latches are to be treated as transparent during modeling.

In contrast, Grodstein does not appear to teach or show locally treating latches as transparent. Rather, Grodstein appears to show a system which *globally* treats latches as transparent. See Grodstein, Col. 1, lines 57-63 and Col. 8, lines 15-38. As Applicants understand Grodstein, the reference does not appear to show any method for providing a delay value to individually treat a latch as transparent as discussed above. As such, the system of Grodstein appears to *globally* assert latch transparency instead of "allowing *a selected subset* of one or more latches of the circuit design to exhibit latch transparency," as recited in Applicants' claim 1. Grodstein further appears to show that *all* latches will exhibit transparency during modeling. Grodstein, at Col. 8, lines 18-19, states "some latches will be transparent once per clock cycle, some several times." Grodstein goes on to describe the frequency with which *all* latches become transparent. See, for example, Grodstein, Col. 8, lines 29-38. As such, Grodstein does not appear to show a method that "allow[s] a selected subset of one or more latches of the circuit design to exhibit latch transparency," as recited in independent claim 1.

Further, Applicants respectfully submit Grodstein does not appear to show "allowing a selected subset of one or more latches of the circuit design to exhibit latch transparency *while the selected subset is still being modeled as non-transparent by the timing tool during modeling*" (emphasis added) as recited in Applicants' claim 1 and similarly in independent claims 18 and 24. Applicants refer

the Examiner to the discussion above regarding the apparent contradiction between exhibiting latch transparency and modeling non-transparence and also to Applicants' Specification at Page 16, lines 5-14. Specifically, Applicants note that while Applicants specification (e.g., FIG. 3) discloses the features of claim 1 of "allowing a selected subset of one or more latches of the circuit design to exhibit latch transparency *while the selected subset is still being modeled as non-transparent by the timing tool during modeling*", Grodstein refers only to latches being transparent during modeling. The FIGS and selected portions of Grodstein referred to by the Examiner (e.g., Col. 8, lines 6+) refer to modeling a latch as transparent, as discussed above. Thus, as Grodstein does not teach or suggest non-transparency, the reference cannot anticipate the present invention.

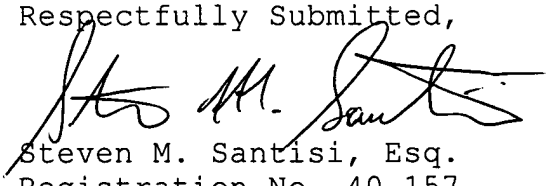
For the above reasons, the Grodstein patent does not appear to disclose "allowing a selected subset of one or more latches of the circuit design to exhibit latch transparency while the selected subset is still being modeled as non-transparent by the timing tool during modeling" as recited by claim 1. Consequently, Applicants respectfully submit claims 1 18, and 24 are not anticipated by Grodstein. Claim 2 depends from independent claim 1, claims 20-23 depend from independent claim 18, and claims 25-31 depend from independent claim 24. Each dependent claim inherits the features of their independent claims and are thus not anticipated by Grodstein either. Accordingly, Applicants respectfully request the Examiner reconsider and withdraw the rejection of these claims.

IV. CONCLUSION

The Applicants believe all the claims to be in condition for allowance, and respectfully request withdrawal of the current rejections and objections.

Applicants do not believe any fees are due in conjunction with this amendment. However, if an Extension of Time is required to make this response timely, please accept this sentence as such a request and charge Deposit Account No. 04-1696 the requisite fee. Applicants do not believe any other fees are due regarding this amendment. If any other fees are required, however, please charge Deposit Account No. 04-1696. The Applicant encourages the Examiner to telephone Applicant's attorney should any issues remain.

Respectfully Submitted,



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